Enclosed is a copy of FIG. 1 of the drawings showing the proposed amendment to FIG. 1 in red ink, along with a new formal drawing for FIG. 1 Applicant respectfully requests that the proposed drawing amendment be approved, and the newly submitted formal drawing be accepted.

With respect to FIG. 6, the Examiner points out that second source/drain 608 is coupled to the trench capacitor 614 and not to first source/drain 604. This is correct, and represents what is claimed in claim 51, what is described in the specification on page 10, line 18 to page 11, line 4, and what is illustrated in FIG. 6. Accordingly, the Applicant submits that FIG. 6 acceptable as is, and respectfully requests removal of the objection to this Figure.

IN THE SPECIFICATION

The specification is amended as follows to add a reference number 110' to identify the first plate as being integral with second source/drain region 110, as described in the specification at page 6, lines 27-28, and as shown in the proposed amended FIG. 1, described above.

The paragraph beginning on page 6, line 26 is amended as follows:

Memory cell 102D also includes storage capacitor 119 for storing data in the cell. A first plate 110' of capacitor 119 for memory cell 102D is integral with second source/drain region 110 of access transistor 111. Thus, memory cell 102D may be more easily realizable when compared to conventional vertical transistors since there is no need for a contact between second source/drain region 110 and capacitor 119. Surface 117 of second source/drain region 110 comprises a "micro-roughened" surface. This micro-roughened surface is formed by coating second source/drain region 110 with poly-silicon and treating the poly-silicon so as to form pores in surface 117. This increases the surface area of second source/drain region 110 and, thus, increases the capacitance of capacitor 119. The pores in surface 117 can be formed, for example, using the etching techniques described below.